# Application Note
## TDK 73M223 to FX604 or MX604 Migration Document

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**Introduction**

The MX604 and FX604 are ultra-low power 1200bps modem integrated circuits that support the V.23 communications protocol and may be used as a replacement for the TDK 73M223. As the MX604 and FX604 are identical they will be referred to in this document as the X604 but pin references given will be for the MX604. For an explanation of the FX and MX prefix please refer to the information in the current Data Sheets.

It has been recently announced that the TDK 73M223 V.23 modem device is to be discontinued. The purpose of this application note is to show how the X604 could be used as a replacement. This application note should be used in conjunction with the MX604 or FX604 data sheets, either of which can be obtained from www.cmlmicro.com/products/datasheets/download.htm.

The X604 can operate from 3.0-5.0 V and can transmit/receive data at 1200bps, half duplex, in the forward channel; it can also transmit data at 75bps via a back channel while simultaneously receiving 1200bps data in the forward channel. The X604 does not necessarily require a micro controller and can also be used in many standalone applications requiring a reliable low-cost modem solution.

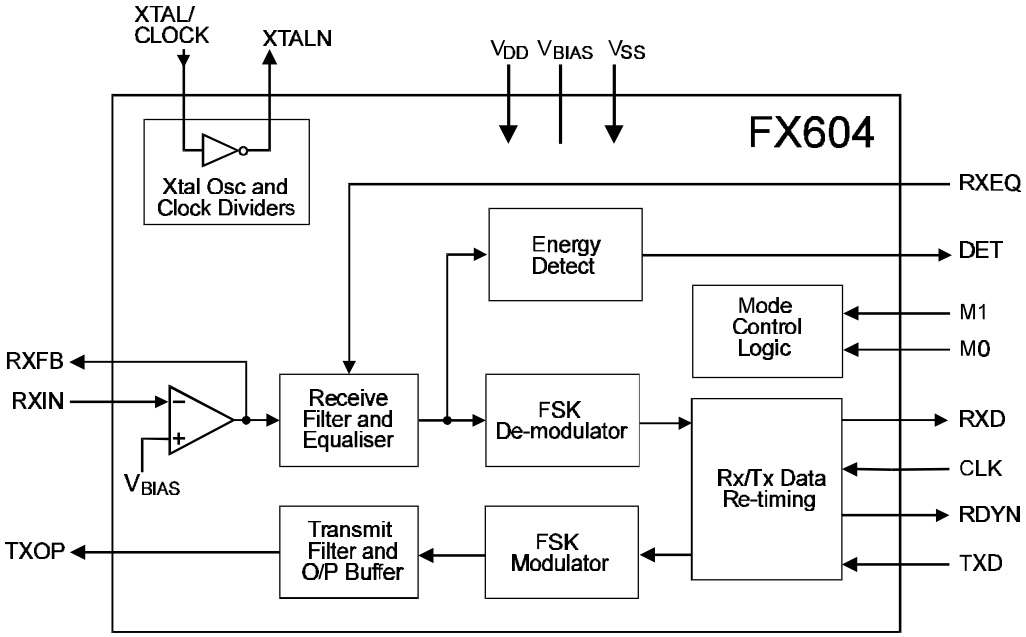


Figure 1 FX604 Block Diagram

**Top Level Comparison**

| Feature | X604 | 73M223 |
|---|---|---|
| 1200bps transmit/receive | Yes | Yes |
| 75bps transmit | Yes | No |
| Line Equalization | Yes | No |
| Data Retiming | Yes | No |
| Carrier Detector | Yes | No |
| Choice of Filtered or Non-Filtered Rx Input | No | Yes |
| 1200Hz output available for system timing | No | Yes |
| Data-synchronized Rx clock output | No | Yes |
| Crystal Frequency | 3.58MHz | 3.18MHz |
| Supply Voltage | 3.0-5.5V | 4.5-13V |
| Power Save " Sleep" Modes | Yes | No |
| Current Consumption (sleep mode) | 1µA | N/A |
| Current Consumption (operating) | 1.0mA typ. @ 3.0V | 2.0mA typ. @ 5.0V |
| Operating temperature | -40°C to +85°C | -25°C to +75°C |
| Dynamic Range | 32dB @ 5V | 15.9dB @ 5V |
| | 32dB @ 3V | 11.5dB @ 3V |
| Voltage Range | 1.13 to 0.028 $V_{pkpk}$ @ 5V | 1.25 to 0.2 $V_{pkpk}$ @ 5V |
| | 0.68 to 0.017 $V_{pkpk}$ @ 3V | 0.75 to 0.2 $V_{pkpk}$ @ 3V |

Table 1 Functional Comparison

**Pin outs**

The following table lists the pin functions for both the X604 and 73M223:

| Pin Number | MX604 | FX604 | X604 Pin Function | 73M223 (PDIP, SOL) |
|---|---|---|---|---|
| 1 | XTALN | $\overline{\text{XTAL}}$ | Output of the on-chip crystal oscillator inverter | $V_{dd}$: Positive supply voltage. |
| 2 | XTAL/CLOCK | XTAL/CLOCK | Input to the on-chip crystal oscillator inverter. | RXA: Receive analogue input from the telephone network. |
| 3 | M0 | M0 | A logic level input for setting the mode of the device. | CAP: Capacitor (0.1uF) between pin 3 and ground. |
| 4 | M1 | M1 | A logic level input for setting the mode of the device. | RXF: Filtered receive analogue input. |
| 5 | RXIN | RXIN | Input to the Rx input amplifier. | FIL: Analogue input control that selects the filtered or non-filtered input. |
| 6 | RXFB | RXAMPOUT | Output of the Rx input amplifier. | TEST: Self-test mode control. |
| 7 | TXOP | TXOUT | Output of the FSK generator. | /TX: Transmitter control. |
| 8 | $V_{SS}$ | $V_{SS}$ | Negative supply (ground) | $V_{ss}$: Ground. |
| 9 | $V_{BIAS}$ | $V_{BIAS}$ | Internally generated bias voltage held at Vdd/2 when the device is not in 'Zero-Power' mode. | SYNC: Synchronous clock output. |
| 10 | RXEQ | RXEQ | Logic level input for enabling/disabling the equalizer in the receive filter. | /SYN: Sync enable. |
| 11 | TXD | TXD | A logic level input for either the raw input to the FSK modulator or data to be re-timed depending on the state of the M0, M1 and CLK inputs. | RXD: Receiver digital output. |
| 12 | CLK | CLK | Logic level input that may be used to clock data bits in/out of the FSK data-retiming block. | TXD: Transmitter digital input. |
| 13 | RXD | RXD | Logic level output carrying either the raw output of the FSK demodulator or re-timed characters depending on the state of the M0, M1 and CLK inputs. | OSC1: Crystal input (3.1872MHz) or external clock input. |
| 14 | DET | DET | Logic level output of the on-chip energy detect circuit. | OSC2: Crystal return. |
| 15 | /RDY | $\overline{\text{RDY}}$ | "Ready for data transfer" output of the on-chip data retiming circuit. | CLK: 1200Hz square wave output. |
| 16 | $V_{DD}$ | $V_{DD}$ | Positive supply rail | TXA: Transmitter analogue output. |

Table 2 Pin Comparisons

**Functional Comparison**

**Timing**

Both the X604 and 73M223 can use clock frequencies outside the specified V.23 compliant crystal frequency (3.579545MHz and 3.18MHz respectively), signaling frequencies will scale accordingly. While

operation with a non-standard timing signal may be advantageous for a particular application, CML Microcircuits does not guarantee the performance of the X604 when operated outside of its published specifications. Also note that filter break points and bandwidths will scale proportionately with the clock. The clock signal levels for the X604 must be at least 40% of $V_{DD}$, peak-to-peak.

The MO and M1 pins are used to select the operating modes. When both MO and M1 are high Zero-Power mode will be selected. If simple logic is used to control the state of these pins (for example placing an inverter between MO and M1 and only driving one pin) then both pins could be placed briefly high, inadvertently selecting Zero-Power mode. This will prevent valid data from being transmitted or received for approximately 20ms and may extend the DET response time.

For X604 operation with an external timing source, pin 1 (XTALN) can be left floating and the crystal oscillator components (X1, C1 and C2) need not be used. If the X604 clock signal is provided by an external source that is not always running, the 'Zero-Power' mode must be set when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by the X604, generate undefined states of the RXD, DET, and /RDY outputs and may damage the device.

The X604 does not require the use of a 1MΩ feedback resistor in the crystal oscillator circuit as does the 73M223.

The 73M223 provides a 1200Hz square wave output on the CLK output (pin 15) that can be used for system timing. The X604 utilises a data retiming system and a serial clock, which means such a dedicated output signal, is unnecessary.

**Transmit/Receive Selection**

The 73M223 transmit signal is enabled by the /TX pin. The 73M223 does not offer a shutdown mode for its receive section.
The X604 provides flexible control of its operating modes with the "Mode Control Logic" pins, M0 (pin 3) and M1 (pin 4). The available modes include:

Transmit at 75bps, Receive at 1200bps
Transmit at 1200bps, Receiver off
Transmitter off, and Receive at 1200bps
'Zero-Power' sleep mode

Note: When applying power to the xX604, the device must be held in the 'zero-power' mode until $V_{DD}$ has stabilized. While in the 'zero-power' mode, all power is removed from the xX604 internal circuitry. When leaving the 'zero-power' mode there must be a minimum of 20ms delay before any Tx data is passed to or Rx data read from the X604. This delay is necessary for the bias level, filters and oscillator to stabilize

**Tx Operating Conditions**

In the 73M223, a logic 0 on the /TX pin activates the transmit output signal. In this condition, logic 1 on the TXD pin will cause a 1302Hz sine wave to be presented on the TXA pin. Likewise, logic 0 on the TXD pin will cause a 2097Hz sine wave to be presented on the TXA pin. No 75bps back channel capability is provided with the 73M223.
The X604 provides transmit output signals for both 1200bps and 75bps operation, depending on the logic condition of the TXD pin and on the state of its Mode Control Logic pins.

For 1200bps operation:

Logic 1 on the TXD pin produces a 1300Hz (<+- 0.25%) tone on the TXOUT pin.
Logic 0 on the TXD pin produces a 2100Hz (<+- 0.14%) tone on the TXOUT pin.

With 75bps operation selected:

Logic 1 on the TXD pin produces a 390Hz (<+- 0.25%) tone on the TXOUT pin.
Logic 0 on the TXD pin produces a 450Hz (<+- 0.22%) tone on the TXOUT pin.

The TXOUT pin is held at approximately $V_{DD}/2$ when the device is placed in the 'zero-power' mode.

Lower data rates when operating synchronously are possible. Any data rate below 1200bps can be used but in this mode the required bit timing must be derived externally. For example it is possible to connect a UART directly to TXD and RXD provided CLK is tied high. The UART will then handle the necessary timing.

**Tx Data Retiming**

In circumstances where a bit is due to be transmitted but the host micro controller is in the middle of handling an interrupt routine, a bit could be sent late and take the transmitter out of specification. The X604 offers a "Tx Data Retiming" feature to assist in this situation. This feature removes the need for the host micro controller to ensure that every data bit is sent to the transmitter once every 833µs (1 bit time at 1200bps). The Tx Data Retiming feature provides a timing 'comfort zone' in which to send the next bit.

**Rx Signal Processing**

The 73M223 allows the user to select whether or not a band pass filter is used to prefilter the incoming data stream. When the band pass filter is to be used, the FIL pin is set to logic 1 and the input signal is applied to the RXF pin. To remove the band pass filter from the signal path, the FIL pin is set to logic 0 and the input signal is applied to the RXA pin. The 73M223 does not provide a user-adjustable input signal amplifier.

The X604 receive filter is an integral part of the internal signal path and cannot be deselected. The X604 also provides an input signal amplifier that can be used to adjust the received signal to the correct amplitude for the FSK receiver and energy detection circuits. The amplifier can also be wired to provide additional simple filtering functions. The 73M223 is AC coupled internally. The X604 can be AC or DC coupled providing correct bias is maintained.

**Rx Equaliser**

The X604 has an internal signal equaliser to adjust the overall group delay of the input signal. The RXEQ pin can enable this equalizer. The 73M223 does not have a signal equaliser.

**Minimum Input Signal Level**

The 73M223 requires a minimum receive signal level of $200mV_{pkpk}$. The X604 minimum receive signal level is approximately $28mV_{pkpk}$, dynamic range is similar.

**Rx Signal Timing**

The 73M223 offers a clock output on the SYNC pin that can be used to either sample the received data stream or be used as a 1200Hz clock. The condition of the /SYN pin determines which of these timing signals are presented on the SYNC pin. The falling edge of the SYNC signal should be used to sample the received data stream. The X604 does not offer clock recovery or a 1200Hz referece.

**Rx Energy Detection**

The DET pin of the X604 offers an in-band energy detector that should be used to qualify the RXD output. The 73M223 does not offer any sort of energy detection indication.

The FSK receiver in the X604 is quite sensitive and in the absence of a valid FSK signal will decode noise as data. This is due to the wideband properties of noise where frequency components of the noise may be present within the FSK decoder's bandwidth.

To prevent spurious reception the DET output is used to determine the validity of the received signal. The detector block is an energy detector that receives predominantly in-band energy from a band-pass filter in the device input. The DET should be monitored during reception and used to 'intelligently' decide whether the data is likely to be valid, suspect or invalid. During periods when there is no data reception the DET will be predominantly low but is likely to false so the receiver should be power saved where practical.
DET does not internally gate the FSK receiver because this would prevent data reception under poor conditions when data recovery may still be possible.

**Rx Data Retiming**

A true UART is not employed in the X604 however a Receive Data Retiming function is. The Rx Data Retiming feature can store nine bits and present them to the uC under the control of strobe pulses applied to the CLK input. The Rx Data Retiming feature reduces the overhead on host devices by permitting a burst read of data, once for every received byte.

**Self Test Mode**

The 73M223 offers an automatic test mode that provides field test capability of the chip's functionality. The X604 does not provide any such functionality.